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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of	:	Howard J. Smith
Serial No.	:	09/945,171
Filed	:	August 30, 2001
For	:	Improved Amplitude and Phase Comparator for Microwave Power Amplifier
Examiner	:	Erin M. File
Art Unit	:	2634
Customer number	:	23644

Declaration Under 37 CFR 131

I, Graham Dolman of 17 Brookhampton Street Ickleton, Saffron Walden, United Kingdom, do hereby declare as follows:

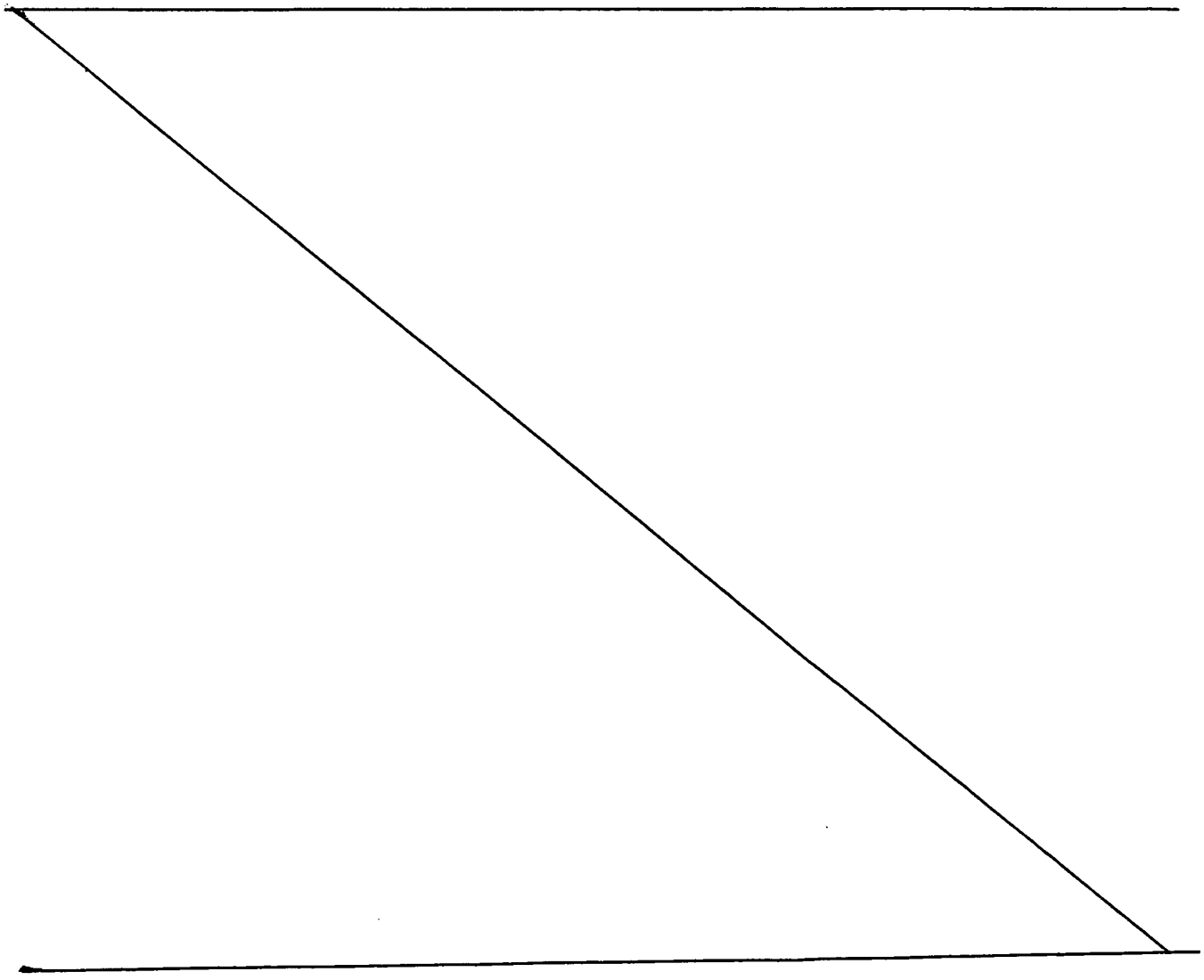
I am one of the inventors and applicants of US Patent Application Serial Number 09/945,171 entitled "Improved Amplitude and Phase Comparator for Microwave Power Amplifier".

Prior to the filing date (August 30, 2001) of the above patent application, I was employed by Nortel Networks UK Limited, a subsidiary of the Assignee of the above patent application Nortel Networks Limited (a Canadian company), together with my colleagues and co-inventors Howard Smith and Scott Widdowson. I can confirm that together we reduced to practice the invention as claimed in the above patent application on or before April 10, 2001.

This reduction to practice is evidenced by the invention disclosure records system of Nortel Networks Limited which contain a "Invention Disclosure Submission Reply" record showing that an Invention Disclosure (ie an internal and confidential disclosure of an invention) having the Nortel internal reference number 14477ID was submitted on April 10,

2001. The Invention Disclosure Submission Reply record includes inventor details, internal Nortel information, summary technical information and an attached document entitled "High Dynamic Range Amplitude Phase Comparator". The attached document is a working paper describing preferred embodiments of the invention in detail, plus variations in summary form and is referenced as "hjsup007_002.doc". Both the Invention Disclosure Submission Reply document and the document entitled "High Dynamic Range Amplitude Phase Comparator" are attached.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.



Signed: 

Name: Graham Dolman

Date: January 20, 2006

Location: Harlow, UK

Advanced Draft - Not Authorised

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UMTS Power Amplifier

High Dynamic Range Amplitude and Phase Comparator

Reference : HJSUP007
Issue : 0.2
Date : 10 April 2001

NORTEL NETWORKS CONFIDENTIAL

	Signature and Date
Howard Smith, Scott Widdowson, Graham Dolman Originators	

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DOCUMENT HISTORY

Issue	Date	Amended by	Sections Changed
0.1	5th April 2001	H.Smith	Whole document - first draft issue
0.2	10th April 2001	H.Smith	Comments incorporated

CONTENTS

LIST OF FIGURES

0. Preface

0.1 Electronic File ID

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0.2 Source data

The basic idea for the amplitude/phase comparator is partially documented in the following places:

1) Howard Smith log book MPA VII, p27, 8 February 2001
2) Graham Dolman Memo GADMP003 issue 0.2, 21 February 2001, section 7.

The DSP algorithm was prototyped by Andy Booth in files ajbmp024.c versions 0.9-0.12, 8th March 2001 to 29th March 2001.

1. Introduction

This working paper describes a novel amplitude and phase comparator system for use in a linearized microwave amplifier system using adaptive predistortion as the linearizing principle.

The predistorter is a signal processing element inserted before the (nonlinear) High Power Amplifier which modifies the input signal with a nonlinearity complimentary to that of the amplifier. On passing through the High Power Amplifier the predistortion sidebands on the modified signal and the distortion products from the amplifier cancel each other, giving a greatly improved output spectrum. This has an advantage over the traditional feedforward linearization architecture in that the signal processing is all carried out on a small signal at the amplifier input, resulting in great savings in cost and power consumption.

However, to achieve more than a few dB reduction in adjacent channel regrowth, the predistorter typically needs to be made adaptive. In this way the predistorter can be continuously adjusted to maintain high performance even as the amplifier response varies with temperature, operating frequency, power supply and aging.

One of the crucial parts of an adaptive predistorter system is a system which estimates the error between the ideal (input) signal and the corrupted system output in order to drive the adaptation process. Depending on the characteristics of the signal, estimating this error to the required degree of accuracy may be extremely challenging. The performance of the error detector system may in fact be limiting on the level of regrowth suppression achievable.

This document describes an amplitude and phase comparator suitable for use as the error detector in a digitally adapted predistorter system. The main advantages of this over previous options can be summarized as follows:

low cost
very economical use of hardware
wide signal bandwidth capability
excellent accuracy even with a high dynamic range signal
adjustment free operation
immunity to temperature and aging
possibility of adding active offset control to stabilize baseband processing

2. Description

2.1 Operating Principle

The purpose of the amplitude and phase comparator is to take two RF signals, sampled from the input and output of a High Power Amplifier system, and to compute amplitude and phase error metrics as a function of the input signal envelope. These metrics can then be used by an adaptation algorithm to adjust the predistortion system.

The comparator is targeted at systems employing CDMA-based modulation formats such as UMTS. Typically such signals have a high variation in the AM power envelope and a wide signal bandwidth. When applied to a non-linearized High Power Amplifier the high AM envelope variation results in an unnacceptable level of distortion products being generated in the adjacent channel. Meanwhile, the high signal bandwidth may make error detection schemes using direct digitization of the system input and output unattractive.

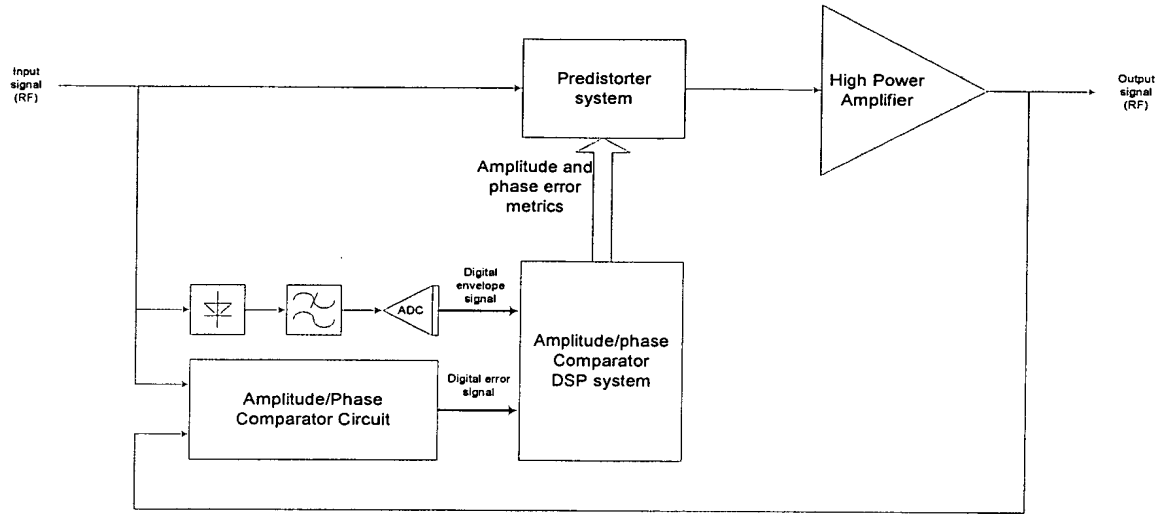
The amplitude and phase comparator system proposed comprises an analogue circuit section and a Digital Signal Processing (DSP) section. The analogue circuit takes two RF inputs, one from the system input and one from the system output. Under the control of the DSP, it produces a signal indicative of the approximate amplitude or phase error between the two inputs as a function of time. The approximate error signal is digitized by the DSP system, along with another digital input relating to the amplitude envelope of the input signal.

In this invention, the DSP captures the digitized error signal in bursts and sorts the data samples using the envelope signal to build up a histogram of error data at each envelope value. The DSP toggles a control line to the analogue circuit which inverts its polarity of operation, then captures another histogram of data. By subtracting and digitally averaging the two sets of data, offsets and nonlinearities in the analogue detector circuit can be cancelled and a much more accurate error metric obtained.

By toggling another control, the DSP can modify the analogue circuit to respond to either amplitude or phase errors. In this way, accurate error metrics can be obtained for both amplitude and phase distortion effects in the High Power Amplifier.

Figure 1 shows an example application for the amplitude/phase comparator in an adaptive predistortion amplifier. A practical design would require additional delay lines, sampling couplers and attenuation elements to present the two RF inputs to the comparator in a nominally equal amplitude, phase and delay relationship.

Figure 1 – Amplitude/Phase Comparator example application



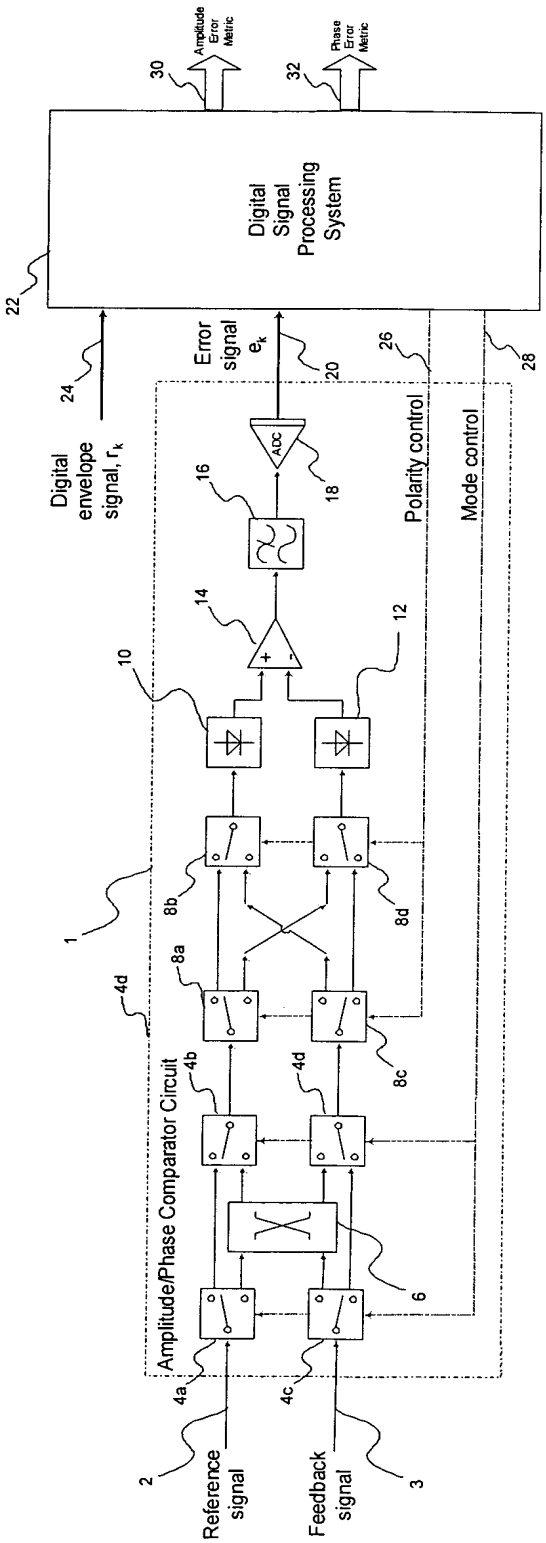
The novel features of the amplitude/phase comparator are:

dual mode amplitude/phase operation
hybrid analogue/digital chopping scheme to cancel offsets and detector nonlinearity
use of digital averaging to improve error SNR

2.2 Amplitude/Phase Comparator Circuit

Figure 2 shows a block diagram of the amplitude/phase comparator circuit.

Figure 2 – Amplitude/Phase Comparator Circuit



The circuit (1) receives two RF inputs, one sampled from the (ideal) input signal (2) and one sampled from the nonlinear output (3). The two signals (2,3) are required to be time aligned at the input to the comparator circuit. The signals (2,3) are applied to an arrangement of four electronic analogue changeover switches (4a, 4b, 4c, 4d) and a 90° hybrid coupler (6). The electronic switches would typically be implemented as monolithic GaAs switches or PIN switches in an implementation.

Depending on the sense of a digital control signal (28) the switches (4a, 4b, 4c, 4d) may be arranged in one of two configurations: to pass signals (2) and (3) directly to subsequent switches (8a, 8c), or to pass them first through a 90° hybrid (6).

The outputs of switches (4b, 4d) are passed to a further arrangement of electronic analogue changeover switches (8a, 8b, 8c, 8d). These are connected in a commutator arrangement so that depending on the sense of a digital control signal (26) the outputs of switches (4b) and (4d) may be passed directly to envelope detectors (10) and (12) respectively or may be swapped over before connecting to these detectors.

The two envelope detectors (10,12) are nominally identical circuits which detect the RF envelope of the signals from switches (8b) and (8c). The resulting baseband signals are fed to a differential amplifier (14) where they are subtracted. The resulting error signal is fed to an analogue-to-digital converter (ADC) (18) via an anti-alias filter (16). The output of the ADC is a sequence of error samples (20), here designated e_k, which is captured by a Digital Signal Processing (DSP) system (22).

In addition, the DSP system (22) captures a digital signal (24), designated r_k, which is indicative of the amplitude of the input signal (2). In a system this could be generated by a separate amplitude detector and ADC as shown in Figure 1, or possibly be supplied directly from the external DSP system used to generate the RF signal input to the amplifier.

The DSP system (22) cycles the amplitude/phase comparator circuit (1) through all four combinations of the polarity (26) and mode (28) control signals. It performs a computation detailed in the next section (see section 2.3) to generate amplitude and phase error metrics (30, 32) which are used by an adaptation system to adjust the predistorter response in the host system.

In the amplitude detection mode of the circuit (switches 4a,4b,4c,4d as shown) the inputs (2), (3) are fed directly, or swapped over, to amplitude detectors (10) and (12). The error signal (20) is then simply proportional to the difference in the amplitude envelope of the input signal (2), (3) assuming ideal envelope detectors. If we denote the input signals (2), (3) in phasor representation as the vectors $\underline{\mathbf{r}}$ and $\underline{\mathbf{f}}$ respectively then the error signal (20) will be given in the ideal case by:

$$\text{Error signal } e_k \propto \pm(\,|\,\underline{\mathbf{r}}\,| - |\,\underline{\mathbf{f}}\,|\,)$$

The sign of the error depends on the sense of the polarity control (26). In general the responses of the detectors (10,12) will be non ideal and non-identical, furthermore the

differential amplifier (14) will typically have a significant d.c. offset. Therefore a real amplitude error signal will be given by:

$$\text{Error signal } e_k \propto +(|\underline{\mathbf{r}}| - |\underline{\mathbf{f}}|) + f_1(|\underline{\mathbf{r}}|) - f_2(|\underline{\mathbf{f}}|))$$

in one state of signal (26), and

$$\text{Error signal } e_k \propto -(|\underline{\mathbf{r}}| - |\underline{\mathbf{f}}|) + f_1(|\underline{\mathbf{f}}|) - f_2(|\underline{\mathbf{r}}|))$$

in the other state of signal (26).

The terms $f_1(|\cdot|)$ and $f_2(|\cdot|)$ are unknown functions of the input envelopes summarizing the offsets, tracking errors and non-ideality of detectors (10,12).

If the raw error signal (20) is used directly to drive the adaptation process, the adaptation will adjust the predistorter response to try and null signal (20) to zero i.e. a flat line. To do this the actual amplitude response between the system input and output ($|\underline{\mathbf{r}}| - |\underline{\mathbf{f}}|$) will converge to $-(f_1(|\underline{\mathbf{r}}|) + f_2(|\underline{\mathbf{f}}|))$ at all envelope values over the dynamic range of the input signal. The functions $f_1(|\underline{\mathbf{r}}|)$ and $f_2(|\underline{\mathbf{f}}|)$ will therefore impose an unwanted distortion term on the predistorter and degrade its performance.

A dramatic improvement can be achieved if the DSP (22) captures two sets of error data from the two states of polarity control (28). For each value of signal envelope as determined by signal (24), the DSP subtracts the error data acquired in one state of signal (26) from that acquired in the other state. As $|\underline{\mathbf{r}}|$ is approximately equal to $|\underline{\mathbf{f}}|$ the wanted error term ($|\underline{\mathbf{r}}| - |\underline{\mathbf{f}}|$) will be reinforced whilst the unwanted error terms due to $f_1(|\cdot|)$ and $f_2(|\cdot|)$ will cancel. In the limit as the predistortion accuracy improves, $|\underline{\mathbf{r}}| \rightarrow |\underline{\mathbf{f}}|$ and the effect of $f_1(|\cdot|)$ and $f_2(|\cdot|)$ is eliminated altogether.

The improvement in spurious performance due to chopping the polarity of the detector provides rejection of imbalances and offsets throughout the baseband chain from the detectors (10,12) up to and including to those arising in the ADC (18). In particular, the response of detectors (10,12) need only track over the power envelope as required to compress the dynamic range of the error signal (20) to a manageable amount.

Without the chopping action, if the baseband circuits are not perfectly balanced it may be necessary to adjust an aiming point in the adaptation loop to optimize the performance of the ampltude/phase detector. With the chopping action in place, the best aiming point is automatically zero and the need for an adjustment is eliminated.

The above discussion describes the action of circuit (1) as an amplitude comparator. It remains to discuss the action of the circuit as a phase comparator.

To select phase operation, control signal (28) is set to the opposite state to that used for amplitude. This inserts hybrid (6) between signals (2) ,(3) and the commutating arrangement (8a, 8b, 8c, 8d). It can be shown that if the amplitude distortion is perfectly corrected so that $|\underline{\mathbf{r}}| = |\underline{\mathbf{f}}|$, then the error signal (20) assuming ideal linear detectors is then

Error signal $e_k \propto |\underline{\mathbf{r}}|.(\sqrt{(1+\sin(\tfrac{1}{2}(\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}))}) - \sqrt{(1-\sin(\tfrac{1}{2}(\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}))})$

This function is periodic with respect to the phase error ($\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}$), and has a period of 2π with a positive-going zero crossing at ($\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}$)=0 and a negative-going zero crossing at ($\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}$)= π. Although it scales linearly with $|\underline{\mathbf{r}}|$, as the zero crossing points where e_k=0 depend only on the phase error ($\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}$), it is a perfectly adequate error signal if all we wish to know is when the two inputs have the same phase.

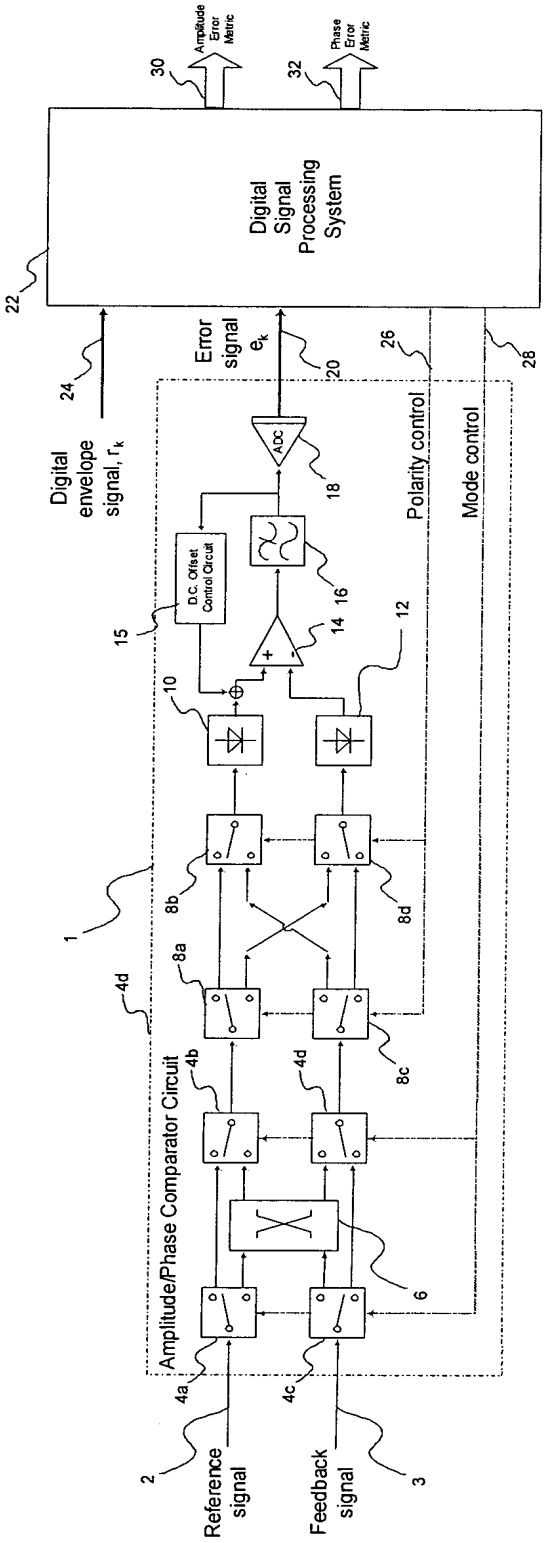
If the adaptation loop operates to drive signal (20) to zero over the full envelope range then the system will be converged when the dynamic phase error ($\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}}$) between the system input and output is constant at zero or π radians (depending on the sign of the adaptation loop). In this condition the phase response is perfectly linearized. The dependency of the error signal on the input signal envelope $|\underline{\mathbf{r}}|$ will effect the dynamics of the adaption loop, however it will not affect the phase relationship at which the comparator indicates a zero phase error.

(If detectors (10,12) are implemented as square law detectors, a somewhat simpler error function $e_k \propto |\underline{\mathbf{r}}|^2.\sin(\angle\underline{\mathbf{r}} - \angle\underline{\mathbf{f}})$ results. The architecture chosen functions just as well if this is the case).

Analogous to the amplitude detector, imbalances and offsets in the detectors (10,12) and baseband circuitry will result in error terms which degrade the accuracy of the phase comparator. By inverting the polarity of the detection circuit (1) and applying an appropriate computation these error terms can again be cancelled to provide an improved phase metric.

There is an additional advantage of this architecture. In implementing a basic amplitude/phase comparator circuit, if a very high amount of baseband gain is required it may prove difficult to stop temperature dependent offsets in the differential amplifier (equivalent to (14) in this invention) being amplified up and overdriving the ADC (equivalent to (18)). As the improved amplitude/phase comparator inherently suppresses offsets in the baseband circuitry, it is possible to add an active d.c. offset control circuit as shown in Figure 3. The indeterminate analogue d.c. offset added by the control circuit (15) is rejected by the chopping action of the detection, wheras in a simple detector it would fatally degrade the accuracy of the circuit.

Figure 3 – Amplitude/Phase comparator circuit with active d.c. offset control



2.3 DSP computation

The DSP processes the error data captured from the error comparator circuit to produce improved amplitude and phase error metrics. These metrics consist of stored arrays of averaged and corrected amplitude and phase errors where the index of the arrays relates to the envelope of the signal.

Prior to processing, the approximate error signal (20) and envelope signal (28) are required to be time aligned by application of appropriate delay elements if necessary. The description here assumes this has been carried out prior to computation.

Referring to Figure 2 the envelope signal (24) is quantized to produce a sequence of indices r_k from 0 to a maximum value r_max. These indices correspond to values of the input signal amplitude envelope at which the average amplitude and phase error due to distortion in the amplifier system is to be evaluated.

To process the amplitude error data, the DSP system executes the process shown in Figure 4. A set of N samples of error data is captured, sorted by envelope, accumulated and stored using the histogram capture process shown in Figure 5. The polarity of the comparator circuit is toggled and another set of error data is captured, accumulated and stored.

For each value of the envelope index, the sum of the stored negative signed errors from the second capture is subtracted from the sum of the positive signed errors from the first capture. The result is then divided by the total error count from both captures. This gives an estimate of the average amplitude error at the envelope value corresponding to that index which is is corrected for systematic offsets and nonlinearities arising in the detector circuit. If the total count for a particular envelope value is zero, then the result of the 0÷0 calculation should be taken as zero.

For phase detection, a similar process is used: see Figure 6.

The outputs of the comparator system are the error metric arrays here denoted as:

Amplitude metric:	err_am(r)
Phase metric:	err_pm(r)

where r is an index relating to the signal envelope, limits 0 to r_max.

Figure 4 – Magnitude error computation

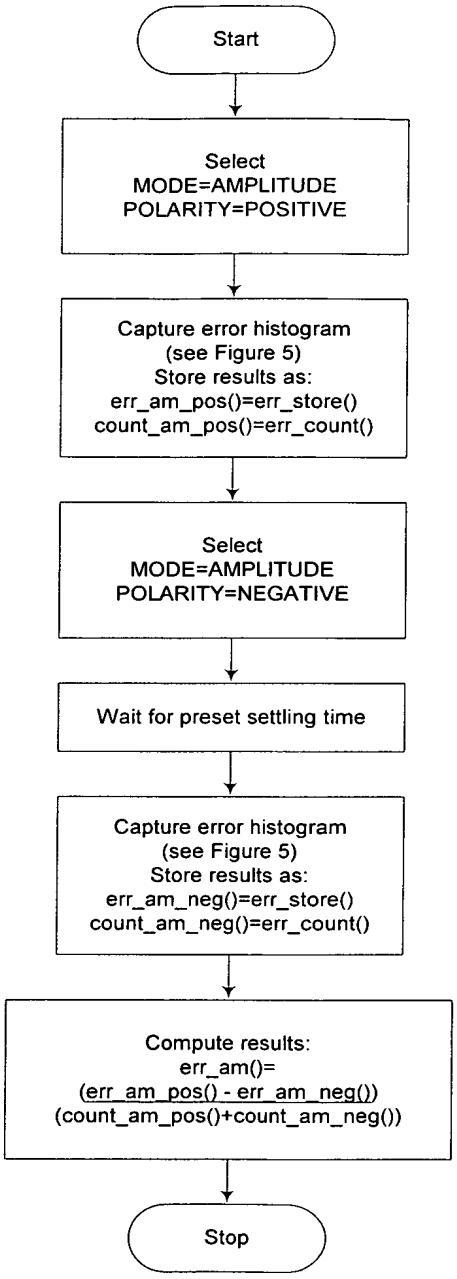


Figure 5 – Histogram capture computation

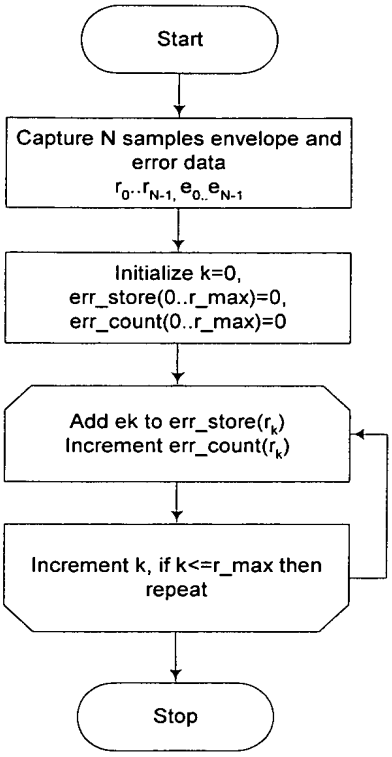
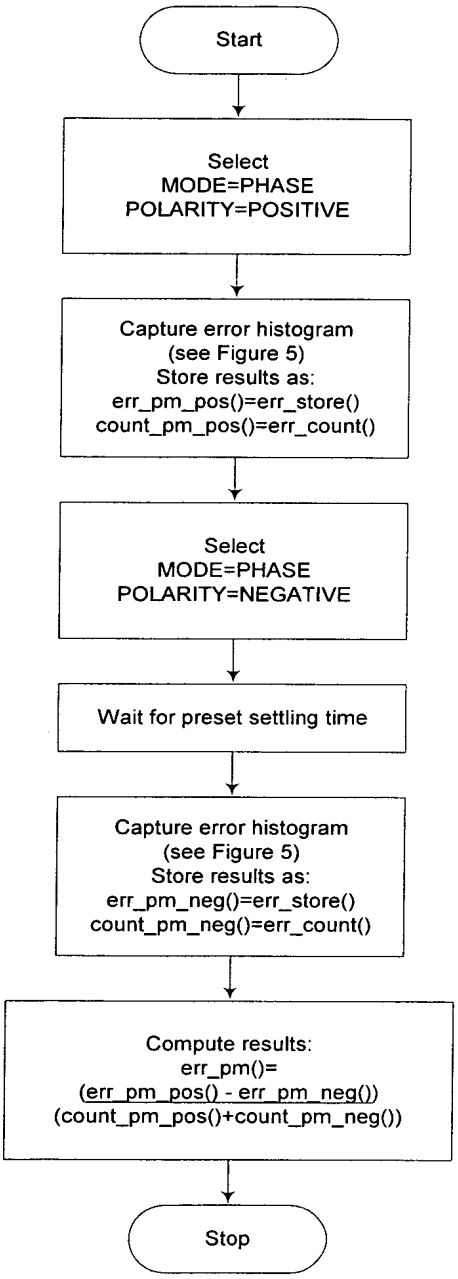


Figure 6 – Phase error computation



3. Variations

A number of variations on the basic scheme are possible.

3.1 DSP variations

3.1.1 Capture sequencing

One possible variation is to re-order the sequence of captures. The version documented here has the following capture sequence:

Amplitude, positive polarity
Amplitude, negative polarity
Phase, positive polarity
Phase, negative polarity

The system would work equally well with the sequence reordered as follows:

Amplitude, positive polarity
Phase, positive polarity
Amplitude, negative polarity
Phase, negative polarity

In fact any order of sequencing would work, although any benefits to doing this are likely to be marginal.

3.1.2 Computation of metrics

The algorithm documented above computes the final metric for each envelope index as:

$$\text{Error metric} = \frac{\{\text{sum of positive signed errors}\} - \{\text{sum of negative signed errors}\}}{\{\text{sum of error count from both captures}\}}$$

This ensures that each sample of error information has an equal 'weight' in the final metric, for a given envelope.

It is also possible to average the positive and negative signed errors individually, and then average the two together:

$$\text{Error metric} = 0.5 * \left(\frac{\{\text{sum of positive signed errors}\}}{\{\text{positive error count}\}} - \frac{\{\text{sum of negative signed errors}\}}{\{\text{negative error count}\}} \right)$$

(In both cases the divisions have to be done intelligently, to resolve any $0 \div 0$ calculations as a result of zero.)

In the case of the second calculation, the key benefits of the comparator in rejecting offsets and detector nonlinearity are still realized so long as a large error count is achieved for both the positive and negative error captures. However, if the error count at a particular envelope index were (for example) 4 for the positive capture but only 1 for the negative capture, then the negative error data sample would be weighted four times higher than each of the 4 positive error samples. In the presence of any patterning effects in the data (such that for some indices, a positive error capture consistently scores a higher or lower count than the negative capture a fixed interval later) this would compromise detector accuracy.

Another variation of the above would involve using a piece of error data for adaptation only if a non-zero count is achieved on both positive and negative captures. This would guarantee at least some cancellation of offset/nonlinearity on all error data used. However, in low-probability regions of the signal probability density function, imposing this condition does greatly decrease the update rate achieveable.

Depending on the adaptation algorithm which uses the metrics, another possibility is to let the adaptation algorithm itself combine the positive and negative error captures. In this case, on one adaptation cycle of the predistorter, the amplitude/phase comparator captures a positive polarity set of error data, divides the sum of errors at each index by the corresponding count, and passes the result to the adaptation system. On the next cycle of adaptation, the amplitude/phase comparator captures a negative polarity set of data, divides the sums of errors by their corresponding counts, and inverts the data before passing it to the adaptation. The positive and negative error samples are then averaged by the adaptation process. For a look-up table (LUT) based predistorter this could work very well, however it will increase the level of noise injected into each bin of the lookup table.

A possible advantage of averaging in the lookup table is that positive and negative captures could be scheduled on a pseudorandom basis, arranged so that the average number of positive captures is equal to the average number of negative captures. This would reduce susceptibility of the offset/nonlinearity calculation to any data pattern-dependent effects.

Yet another possibility when processing the errors would be to accumulate the error histograms on a rolling basis, rather than resetting each envelope value to zero on each capture. A wide variety of options are possible, these then introduce a time constant into the comparator system but do have the advantage of further reducing the noise on the output error metrics.

All of these methods are feasible, and exhibit a range of different strengths and weaknesses. They all however result in (a) the error data acquired being digitally averaged somewhere in the system (b) combination of data from positive and negative polarity modes of the analogue comparator circuit to suppress offsets and detector nonlinearity/non-tracking.

3.1.3 Normalization of error data

Both the amplitude and phase modes of the comparator have a response approximately proportional to $|\underline{\mathbf{r}}|$, assuming the detectors (10,12) are linear with envelope voltage. Whilst this does not affect the detection of a zero error condition, it will affect the dynamics of the predistorter adaptation over the signal envelope range.

To optimize the adaptation process there may be some merit in normalizing the error metrics, i.e. dividing the errors by $|\underline{\mathbf{r}}|$ (at least approximately) to make the error functions independent of envelope to first order. The difficulty in doing this with a simple amplitude/phase comparator is that of offsets in the baseband chain (14,16,18). As the envelope r_k of the signal becomes small, the error signal e_k becomes increasingly dominated by offsets in the baseband chain. If we simply form a quotient r_k/e_k for each sample the offsets will be amplfied as $r_k \rightarrow 0$ and the error data at low envelopes will become very innaccurate.

With the chopped detector described in this document, the very good intrinsic suppression of d.c. offset makes normalization of the error metric much more feasible. One possibility is to compute the error metric for envelope of index r as follows:

$$\text{Error metric} = \frac{\{\text{sum of positive signed errors}\} - \{\text{sum of negative signed errors}\}}{r * \{\text{sum of error count from both captures}\}}$$

END OF DOCUMENT

Invention Disclosure Submission Reply

Disc No:	14477ID	**Received Date:**	10 apr 2001
Disclosure Title:	AMPLITUDE AND PHASE COMPARATOR FOR MICROWAVE POWER AMPLIFIER		

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		GEORGIA AND THE SOUTH SANDWICH ISLANDS	

---=== Attachments ===---

File Name	File Type	File Comments
hjsup007_002.doc	Microsoft Word (*.doc)	This document is a working paper describing the preferred embodiment in detail, plus variations in summary form

<End of Attachments>

Were there additional inventors involved:	yes	**Was there contractor involvement:**	no
Name of Supervisor or Divisional Head:		**Name of VP:**	
IAN MCCLYMONT		ABDUL KHAWAR	
LOB:	WIRELESS INTERNET	**Business Unit:**	WIRELESS-INTERNET
Conception Date:			
Has this invention been discussed with others? If so, please complete:			
Inside Nortel - Whom?		**Outside Nortel - Whom?**	
Inside Nortel - When?		**Outside Nortel - When?**	
NDA?	no		
Are you aware of any imminent future disclosures? Please provide dates and details:			
Keywords for Searching:		**Products that will use this invention:**	
		Predistortion-based linear microwave power amplifiers aimed at 3G cellular (UMTS). Invention is key to power amplifier product development for the NMC UMTS iBTS.	
Does this invention arise from any arrangement involving an external organization?	no		
Is this invention relevant to a Standards Activity?		**Internal Funding Project #'s:**	
no		17537, 30033	

Technical Information

Brief Description of the Invention:

This document describes a highly accurate amplitude and phase comparator suitable for use as the error detector in a digitally adapted predistorter system.

The purpose of the amplitude and phase comparator is to take two RF signals, sampled from the input and output of a High Power Amplifier system, and to compute amplitude and phase error metrics for adapting a predistortion system inserted before the High Power Amplifier. The function of the predistorter is to compensate for nonlinear effects in the amplifier, thus improving the output spectrum as required by the regulatory specifications. The accuracy of the comparator is crucial for achieving this goal.

Problem Solved by the Invention:

The main advantages of this over previous options can be summarized as follows:

low cost
very economical use of hardware
wide signal bandwidth capability
excellent accuracy even with a high dynamic range signal
adjustment free operation
immunity to temperature and aging
possibility of adding active offset control to stabilize baseband processing

The amplitude/phase comparator is a key enabler to implementing the technique of digital adaptive predistortion in the power amplifier. Predistortion is a recent technique made possible by advances in DSP technology which dramatically reduces the cost and power consumption of linear power amplifiers.

Solutions that have been tried and why they didn't work:

The default option is to use two separate circuits for amplitude and phase detectors, without polarity inversion. This has the following disadvantages:

approximately twice as much circuitry -> high cost
poor accuracy
needs adjustment
performance degrades over temperature and ageing
any attempt to stabilize offset voltage using active control is likely to degrade performance further

Specific elements or steps that solved the problem and how they do it:

The invention comprises an analogue circuit section and a Digital Signal Processing (DSP) section. The analogue circuit takes two RF inputs and under control of the DSP, it produces a signal indicative of the approximate amplitude or phase error (depending on mode) between the two inputs as a function of time.

The DSP captures the digitized error signal along with an envelope signal and sorts the data samples to build up a histogram of error data at each envelope value. The DSP toggles a control line to the analogue circuit which inverts its polarity of operation, and captures another histogram of data. By subtracting and digitally averaging the two sets of data, offsets and nonlinearities in the analogue detector circuit can be cancelled and a much more accurate error metric obtained.

By toggling another control, the DSP can modify the analogue circuit to respond to either amplitude or phase errors. In this way, accurate error metrics can be obtained for both amplitude and phase distortion effects in the High Power Amplifier.

Commercial value of the invention to Nortel and Nortel's major competitors:
This invention makes it possible to reliably meet UMTS specifications in a power amplifier linearized using the adaptive predistortion technique. Relative to the prior art feedforward design, this allows a $3000 amplifier to be cost reduced to approx $2000. On an estimated $25k units per year, the cost saving is $25m per year.